AN-1001
Understanding Power MOSFET Parameters
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MOSFET datasheet parameters introduction

Introduction

When choosing a MOSFET, parameters that are focused on by most engineers intuitively are $V_{DS}$, $R_{DS(on)}$, $I_D$. However, in power systems, it is significant to pick up a suitable MOSFET based on different applications. In this application note, Taiwan Semiconductor (TSC) introduces the definition of every single parameter of a MOSFET, and from chapter 3, TSC also explains how each parameter is realized, hoping this would help designers on the power projects.

1. Absolute Maximum Ratings

| ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted) |
|-----------------------------|--------------|-------|----------|
| PARAMETER                      | SYMBOL | LIMIT | UNIT   | Notes |
| Drain-Source Voltage          | $V_{DS}$ | 30    | V      | 1.1    |
| Gate-Source Voltage           | $V_{GS}$ | ±20   | V      | 1.2    |
| Continuous Drain Current      | $I_D$   | 11    | A      | 1.3    |
| (Note 1) $T_C = 25^\circ C$   |         |       |        |        |
| (Note 1) $T_A = 25^\circ C$   |         |       |        |        |
| Pulsed Drain Current          | $I_{OM}$ | 156   | A      | 1.4    |
| Single Pulse Avalanche Current| $I_{AS}$ | 15.6  | A      | 1.5    |
| (Note 2)                      |         |       |        |        |
| Single Pulse Avalanche Energy | $E_{AS}$ | 36.5  | mJ     | 1.6    |
| (Note 2)                      |         |       |        |        |
| Total Power Dissipation       | $P_D$   | 33    | W      | 1.7    |
| ($T_C = 25^\circ C$)          |         |       |        |        |
| ($T_C = 125^\circ C$)         |         |       |        |        |
| Total Power Dissipation       | $P_D$   | 2.6   | W      | 1.7    |
| ($T_A = 25^\circ C$)          |         |       |        |        |
| ($T_A = 125^\circ C$)         |         |       |        |        |
| Operating Junction and Storage Temperature range | $T_J$, $T_{STG}$ | -55 to +150 | °C | 1.8 |

1.1 Drain-Source Voltage ($V_{DS}$)

$V_{DS}$ represents MOSFET absolute maximum voltage between Drain and Source. In operations, voltage stress of Drain-Source should not exceed maximum rated value.

1.2 Gate-Source Voltage ($V_{GS}$)

$V_{GS}$ represents operating driver voltage between Gate and Source. In operations, voltage stress of Gate-Source should not exceed maximum rated value.

1.3 Continuous Drain Current ($I_D$)

$I_D$ represents MOSFET’s continuous conduction current and could be calculated by below equation.

$$I_D = \frac{T_J - T_C}{R_{\theta JC} \times R_{DS(on)} \times K}$$

$T_J$ = Junction Temperature
$T_C$ = Case Temperature
$R_{DS(on)}$ = Drain-Source On-State Resistance
$R_{\theta JC}$ = Junction to Case Thermal Resistance
$K$ = On-Resistance vs. Junction Temperature
1.4 Pulsed Drain Current (\(I_{DM}\))

\(I_{DM}\) represents maximum limit current in MOSFET SOA (Safe Operating Area). A MOSFET could be well operated within SOA to make sure the stability and safety of a power system.

1.5 Single Pulse Avalanche Current (\(I_{AS}\))

When power MOSFET enters the avalanche mode, the current transformed into the form of voltage across Drain and Source of a MOSFET is called avalanche current (\(I_{AS}\)).

1.6 Single Pulse Avalanche Energy (\(E_{AS}\))

UIL (unclamped inductive load) or UIS (unclamped inductive switching) tests are important to check the degree of robustness of a power MOSFET. \(E_{AS}\) represents allowed maximum energy in either one pulse that is over rated \(V_{DS}\). When the operating voltage exceeds the specified \(V_{DS}\) at off state of a MOSFET, it will enter the avalanche mode and cause high power dissipation. The parameter is often taken into consideration when inductive load or transient loading is operated.

\[
E_{AS} = \frac{1}{2} \times L \times I_{AS}^2 \times \left(\frac{BV_{DS}}{BV_{DS} - V_{DD}}\right)
\]

The UIS test circuit: When applying a \(V_{GS}\) signal to a DUT and the DUT is turned on, the current will start to charge Inductor (L), phenomenon of the \(I_0\) current rising rate behaves linearly as above picture. When the required \(I_0\) is reached to \(I_{AS}\), the DUT is then turned off, causing the Inductor to dissipate all of its stored energy and enforcing the DUT to reach its breakdown voltage rating. The DUT will remain in breakdown (\(BV_{DS}\)) until all of the energy is dissipated. The blue area is \(E_{AS}\) (Energy Avalanche Single).
1.7 Total Power Dissipation (P_D)

P_D represents the capability of maximum power dissipation that a MOSFET can handle. Moreover, capability of power dissipation varies by different temperature conditions.

When case temperature (T_C) is considered, equation would be:

\[
P_D = \frac{T_J - T_C}{R_{\theta JC}}
\]

As for ambient temperature (T_A), equation turns into:

\[
P_D = \frac{T_J - T_A}{R_{\theta JA}}
\]

T_J = Junction Temperature
T_C = Case Temperature
R_{\theta JC} = Junction to Case Thermal Resistance
R_{\theta JA} = Junction to Ambient Thermal Resistance

1.8 Operating Junction and Storage Temperature Range (T_J, T_{STG})

T_J represents maximum operating temperature of a MOSFET. A MOSFET should be avoided to be operated over the rated temperature limit.

T_{STG} represents the range of temperature for storage or transportation of a MOSFET. It must be storage in specified temperature values.
2. Thermal Performance

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>LIMIT</th>
<th>UNIT</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction to Case Thermal Resistance</td>
<td>$R_{\theta JC}$</td>
<td>3.8</td>
<td>°C/W</td>
<td>2.1</td>
</tr>
<tr>
<td>Junction to Ambient Thermal Resistance</td>
<td>$R_{\theta JA}$</td>
<td>48</td>
<td>°C/W</td>
<td>2.2</td>
</tr>
</tbody>
</table>

2.1 Junction To Case Thermal Resistance ($R_{\theta JC}$)

$R_{\theta JC}$ is the sum of the junction to case thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.

2.2 Junction To Ambient Thermal Resistance ($R_{\theta JA}$)

$R_{\theta JA}$ is the sum of the junction to case and case to ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.
3. Electrical Specifications

### ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)

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<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>SYMBOL</th>
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<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
<th>Notes</th>
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<tbody>
<tr>
<td><strong>Static</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain-Source Breakdown Voltage</td>
<td>V_GS = 0V, I_D = 250µA</td>
<td>BV_{DSS}</td>
<td>30</td>
<td>--</td>
<td>--</td>
<td>V</td>
<td>3.1</td>
</tr>
<tr>
<td>Gate Threshold Voltage</td>
<td>V_GS = V_DS, I_D = 250µA</td>
<td>V_{GS(TH)}</td>
<td>1.2</td>
<td>1.9</td>
<td>2.5</td>
<td>V</td>
<td>3.2</td>
</tr>
<tr>
<td>Gate-Source Leakage Current</td>
<td>V_GS = ±20V, V_DS = 0V</td>
<td>I_{GSS}</td>
<td>--</td>
<td>--</td>
<td>±100</td>
<td>nA</td>
<td>3.3</td>
</tr>
<tr>
<td>Drain-Source Leakage Current</td>
<td>V_GS = 0V, V_DS = 30V</td>
<td>I_{DSS}</td>
<td>--</td>
<td>--</td>
<td>1</td>
<td>µA</td>
<td>3.4</td>
</tr>
<tr>
<td></td>
<td>V_GS = 0V, V_DS = 30V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_J = 125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain-Source On-State Resistance</td>
<td>V_GS = 10V, I_D = 11A</td>
<td>R_{DS(on)}</td>
<td>--</td>
<td>8.3</td>
<td>11.7</td>
<td>mΩ</td>
<td>3.5</td>
</tr>
<tr>
<td>(Note 3)</td>
<td>V_GS = 4.5V, I_D = 11A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Forward Transconductance</td>
<td>V_DS = 5V, I_D = 11A</td>
<td>g_{fs}</td>
<td>--</td>
<td>35</td>
<td>--</td>
<td>S</td>
<td>3.6</td>
</tr>
</tbody>
</table>

3.1 **Drain-Source Breakdown Voltage (BV_{DSS})**

To measure breakdown voltage of a MOSFET, at first, short Gate pin and Source pin, and then, supply the I_D=250µA, and monitor the reading of V_DS.

![Image of drain-source breakdown voltage](attachment:image)

BV_{DSS} is determined when I_D reaches 250µA. Gate pin is shorted to Source pin.

3.2 **Gate Threshold Voltage (V_{GS(TH)})**

To measure gate threshold voltage of a MOSFET, at first, short Gate pin and Drain pin, and then, with a given I_D=250µA, and monitor the voltage difference between Gate-Source. One significant characteristics of V_{GS(TH)} is its negative temperature coefficient. If power system has to be operated at a certain minus degree, to avoid unpredicted being turned on, V_{GS(TH)} needs to be taken into consideration.

![Image of gate threshold voltage](attachment:image)

V_{GS(TH)} is determined when I_D reaches 250µA. Gate pin is shorted to Drain pin.
3.3 Gate-Source Leakage Current (I_{GSS})

To measure Gate-Source leakage current of a MOSFET, at first, short Drain pin and Source pin, and then, apply maximum allowable voltage on Gate-Source and monitor the leakage current of Gate-Source. I_{GSS} is dependent on the structure and design of the gate oxide.

![Diagram of MOSFET with I_{GSS} measurement](image)

I_{GSS} is determined when maximum V_{GS} voltage is applied. Drain pin is shorted to source pin.

3.4 Drain-Source Leakage Current (I_{DSS})

To measure Drain-Source leakage current of a MOSFET, at first, short Gate pin and Source pin, and then, apply maximum allowable voltage on Drain-Source and monitor the leakage current of Drain-Source.

![Diagram of MOSFET with I_{DSS} measurement](image)

I_{DSS} is determined when maximum V_{DS} voltage is applied. Gate pin is shorted to Source pin.

3.5 Drain-Source On-State Resistance (R_{DS(on)})

To measure Drain-Source on resistance, R_{DS(on)}, at first, apply a voltage across Gate-Source, which is specified to be higher than V_{GS(TH)}. With a given current source, I_D, measure the voltage drop across Drain-Source, V_{DS}. And after that, through the equation, R_{DS(on)} = V_{DS} / I_D, R_{DS(on)} is observed. In TSC MOSFET datasheet, two additional figures are introduced as well. One is R_{DS(on)} vs V_{GS} graph since R_{DS(on)} varies by different amplitude of V_{GS}. The other one is R_{DS(on)} vs T_J. Characteristics of R_{DS(on)} is positive temperature coefficient. It is important to consider the surrounding temperature of selecting a MOSFET in a power system.

![Diagram of MOSFET with R_{DS(on)} measurement](image)

Apply specified V_{GS}, and given I_D, measured V_{DS} of a MOSFET, then R_{DS(on)} is obtained.
3.6 Forward Transconductance ( $g_{fs}$ )

Forward transconductance, $g_{fs}$, represents the signal gain (drain current divided by gate voltage) of a MOSFET. Higher $g_{fs}$ indicates the high current ($I_{DS}$) handling capability can be gained from the low gate voltage ($V_{GS}$). It is also expressed as below equation.

\[
g_{fs} = \frac{\Delta I_{DS}}{\Delta V_{GS}}
\]
4. Dynamic

| Dynamic (Note 4) | $V_{GS} = 10V, V_{DS} = 15V, I_D = 11A$ | $Q_g$ | -- | 9.2 | -- | nC | 4.1 |
|-----------------|-------------------------------------|-------|------|-----|-----|----|
| Total Gate Charge | $V_{GS} = 4.5V, V_{DS} = 15V, I_D = 11A$ | $Q_g$ | -- | 4.5 | -- | -- |
| Gate-Source Charge | $V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz$ | $Q_{gs}$ | -- | 1.9 | -- | -- |
| Gate-Drain Charge | $V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz$ | $Q_{gd}$ | -- | 1.7 | -- | -- |
| Input Capacitance | $V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz$ | $C_{iss}$ | -- | 562 | -- | pF | 4.2 |
| Output Capacitance | $V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz$ | $C_{oss}$ | -- | 144 | -- | -- |
| Reverse Transfer Capacitance | $V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz$ | $C_{rss}$ | -- | 50 | -- | -- |
| Gate Resistance | $f = 1.0MHz$, open drain | $R_g$ | 0.5 | 1.7 | 3.4 | Ω | 4.3 |

4.1 Total Gate Charge ($Q_g$)

Gate charge plays prominently in high frequency switching applications. Total gate charge $Q_g$ includes $Q_{gs}$ and $Q_{gd}$. $Q_{gs}$ represents the accumulation of Gate-Source capacitance while $Q_{gd}$ is the accumulation of Gate-Drain capacitance, also called miller capacitor. In high frequency operations, $Q_g$ should be selected as small as possible. Another tip of Gate charge for picking up a MOSFET in H-bridge power system design is that ratio of $Q_{gd}/Q_{gs}$ be lower than 1 to prevent the circuit from shoot through.

4.2 Capacitances ($C_{iss}$, $C_{oss}$, $C_{rss}$)

$C_{iss}$, $C_{oss}$, and $C_{rss}$, like gate charge, also influence on switching performance. In TSC MOSFET Datasheet, either one would be tested at various Drain-Source voltages and under 1MHz frequency conditions. Relationships of MOSFET capacitances are listed below.

$$ C_{iss} = C_{gs} + C_{gd} $$
$$ C_{oss} = C_{ds} + C_{gd} $$
$$ C_{rss} = C_{gd} $$

4.3 Gate Resistance ($R_g$)

$R_g$ is designed and implemented inside gate area. And with the help of MOSFET embedded $R_g$, the external gate drive circuit could be simplified.
5. Switching time

<table>
<thead>
<tr>
<th>Switching (Note 4)</th>
<th>$V_{GS} = 10V$, $V_{DS} = 15V$, $I_D = 7A$, $R_G = 10\Omega$,</th>
<th>$t_{d(on)}$</th>
<th>--</th>
<th>8.4</th>
<th>--</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn-On Delay Time</td>
<td>$t_r$</td>
<td>--</td>
<td>4.3</td>
<td>--</td>
<td>5.1</td>
</tr>
<tr>
<td>Turn-On Rise Time</td>
<td>$t_{d(off)}$</td>
<td>--</td>
<td>22.4</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>Turn-Off Delay Time</td>
<td>$t_f$</td>
<td>--</td>
<td>3.1</td>
<td>--</td>
<td></td>
</tr>
</tbody>
</table>

### 5.1 Switching Time ( $t_{d(on)}$, $t_r$, $t_{d(off)}$, $t_f$ )

Switching time includes $t_{d(on)}$, $t_r$, $t_{d(off)}$, and $t_f$ four main parameters and also represent important impact on switching loss of MOSFET. Each one is described as below.

$t_{d(on)}$ – Turn-on Delay Time
The turn-on delay time is defined as the time interval measured between 10% of $V_{GS}$ rising from zero and 90% of $V_{DS}$ falling from rated voltage.

$t_r$ – Rise Time
$t_r$ represents the time interval between $V_{DS}$ falling from 90% to 10% of rated voltage. $I_D$ starts to rise and is considered to be the major turn-on losses during this period.

$t_{d(off)}$ – Turn-off Delay Time
The turn-off delay time is defined as the time interval measured between 10% of $V_{DS}$ rising from zero and 90% of $V_{GS}$ falling from rated voltage.

$t_f$ – Fall Time -
$t_f$ represents the time interval between $V_{DS}$ rising from 10% to 90% of rated voltage. $I_D$ starts to fall and is considered to be the major turn-off losses during this period.

![Diagram showing the relationship between $V_{DS}$ and $V_{GS}$ with $t_{d(on)}$, $t_r$, $t_{d(off)}$, and $t_f$.]
6. Source-Drain Diode Characteristics

<table>
<thead>
<tr>
<th>Source-Drain Diode</th>
<th>Forward Voltage (Note 3)</th>
<th>$V_{GS} = 0V$, $I_S = 11A$</th>
<th>$V_{SD}$</th>
<th>--</th>
<th>1.2</th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse Recovery Time</td>
<td>$I_S = 11A$, $dI/dt = 100A/\mu s$</td>
<td>$t_{rr}$</td>
<td>--</td>
<td>14.7</td>
<td>--</td>
<td>ns</td>
</tr>
<tr>
<td>Reverse Recovery Charge</td>
<td>$dI/dt = 100A/\mu s$</td>
<td>$Q_{rr}$</td>
<td>--</td>
<td>7.3</td>
<td>--</td>
<td>nC</td>
</tr>
</tbody>
</table>

6.1 Forward Voltage ($V_{SD}$)

To measure Source-Drain voltage, $V_{SD}$, at first, short Gate pin and Source pin. Apply a specified reverse current, $I_S$, and $V_{SD}$ is measured.

![Diode Circuit Diagram](image)

The $V_{SD}$ is measured by applying $I_S$ current. Gate pin is shorted to Source pin.

6.2 Body Diode Reverse Recovery ($t_{rr}$, $Q_{rr}$)

To measure reverse recovery time, $t_{rr}$ and reverse recovery charge, $Q_{rr}$, at first, short Gate pin and Source pin of DUT MOSFET. Moreover, a gate drive circuit, a given voltage source, $V_{dd}$, and an inductor are required to form a diode recovery test circuit. When MOSFET of gate drive circuit is turned on, $L$ is charged; when it is turned off, energy of inductor will be discharged through intrinsic body diode of DUT MOSFET. When MOSFET of gate drive circuit is turned on again, the body diode of DUT will be reversed biased and reverse recovery starts to behave. $t_{rr}$ and $Q_{rr}$ are measured.

![Diode Recovery Test Circuit Diagram](image)

t_{rr} and $Q_{rr}$ are measured through above test circuit. Short Gate pin and Source pin of DUT MOSFET in applications, when $I_{SD}$ reaches back to zero, the voltage spike happens on Drain-Source due to inductor energy released to $C_{oss}$ of MOSFET. Higher $Q_{rr}$ would cause severe voltage spike and vice versa.
7. Characteristics Curves
(T_A = 25°C unless otherwise noted)

**Output Characteristics**

\[ V_{DS} = V_{GS} - V_{GS(TH)} \]

In output characteristics, three major regions are introduced: Ohmic region, Linear region, and Cutoff region. The figure also shows the curve defined by \( I_D \) vs \( V_{DS} \) at various gate to source voltage conditions. When MOSFET is turned on with \( V_{GS} < V_{GS(TH)} \), it is operated in cutoff region. When \( V_{DS} > V_{GS} - V_{GS(TH)} \), it is operated at linear region. Finally, when \( V_{DS} < V_{GS} - V_{GS(TH)} \), it is operated in Ohmic region. The blue dash line is defined by \( V_{DS} = V_{GS} - V_{GS(TH)} \).

**Transfer Characteristics**

The transfer characteristics curve represents both \( V_{GS} \) and \( I_D \) relationship. From above, there is a ZTC point (Zero Temperature Coefficient). If \( V_{GS} \) is under ZTC point, \( V_{GS} \) becomes a negative temperature coefficient and vice versa.
Gate charge include 3 specified values, \( Q_{gs} \), \( Q_{gd} \), and \( Q_{g} \). \( Q_{gs} \) denotes Gate to Source charge. \( Q_{gd} \) denotes Gate to Drain charge, which is also called the miller effect charge. \( Q_{g} \) denotes the total gate charge.

Operations of Gate Charge are presented as below from above diagram.

1. **T0 ~ T1**
   
   When \( V_{GS} \) rises and reaches to \( V_{GS(TH)} \), \( C_{GS} \) is the capacitor to be charged. At the time, both \( I_{D} \) and \( V_{DS} \) present unchanged.

2. **T1 ~ T2**
   
   At this time interval, MOSFET is working in linear region. \( V_{GS} \) continues stepping up to the plateau voltage, \( V_{P} \). \( C_{GS} \) is completely charged and \( I_{D} \) is raised up to full load current.

3. **T2 ~ T3**
   
   At this time interval, MOSFET is still working in linear region. And, \( V_{DS} \) voltage starts to decrease and finally drops to zero. So the \( C_{GD} \) * \( (dV_{DS}/dt) \) becomes big and thus, creates current flowing through \( C_{GD} \), which blocks \( V_{GS} \) keeps rising and maintains constant. During this time, \( R_{DS(on)} \) changes from high impedance to low impedance, entering Ohmic region.

4. **T3 ~ T4**
   
   In this timing, \( V_{GS} \) is raised up to rated value and MOSFET is operated in Ohmic region.
From the curve of $R_{DS(on)}$ vs. $T_J$, it's seen the normalized $R_{DS(on)}$ is 1 at $T_J=25°C$, and 1.85 at $T_J=150°C$. This indicates if the $R_{DS(on)}$ is 12mohm at $T_J=25°C$, it is expected to be 22.2 mohm at $T_J=150°C$.

\[
K = \frac{(K_{150°C} / K_{25°C})}{1} = 1.85 / 1 \Rightarrow 1.85
\]

\[
R_{DS(on)} = 12\text{mohm}
\]

\[
R_{DS(on) - 150°C} = (R_{DS(on) - 25°C} \times K) = 12\text{mohm} \times 1.85 \Rightarrow 22.2\text{mohm}
\]
From above curve, it is easily seen $V_{SD}$ has negative temperature coefficient. So, it is expected to obtain lower $V_{SD}$ voltage at higher temperature. From curve remarked, $V_{SD}$ is 0.5V at $T_J=150^\circ$C; $V_{SD}$ is 0.72V at $T_J=25^\circ$C; $V_{SD}$ is 0.85V at $T_J=-55^\circ$C.

Above curve is $BV_{DSS}$ vs. $T_J$. $BV_{DSS}$ is positive temperature coefficient. Based on above curve, It is seen the normalized $BV_{DSS}$ is 1 at $T_J=25^\circ$C, and 1.09 at $T_J=150^\circ$C. That is, if the $BV_{DSS}$ is 30V at $T_J=25^\circ$C, it is expected $BV_{DSS}$ is 32.7V at $T_J=150^\circ$C.

\[
K = \frac{K_{-150^\circ}C}{K_{-25^\circ}C} = \frac{1.09}{1} \Rightarrow 1.09
\]

\[B \cdot BV_{DSS -150^\circ}C = (BV_{DSS -25^\circ}C \times K) = 30V \times 1.09 \Rightarrow 32.7V\]
MOSFET have three types capacitances, Ciss, Coss and Crss. Regarding to the relationship of these capacitances, VDS voltage and frequency, it is introduced from above curve with a fixed frequency to observe to variations of Ciss, Coss, and Crss. These three capacitances will affect the switching loss of power system. Below shows defined three types capacitances.

MOSFET Equivalent Circuit
SOA is defined the maximum value of \( V_{DS} \), \( I_D \) and time envelope of operation which guarantees safe operation when MOSFET works is actively biased. Four lines are used to determine the maximum operating limits.

**Line 1**

\( R_{DS(on)} \) limits. For example, take TSC 30V MOSFET as example, whose maximum \( R_{DS(on)} \) is 11.7 mohm. According to the ohm’s law, when \( V_{DS} \) is 1.0V and \( R_{DS(on)} \) is 11.7 mohm. \( I_D = \frac{1.0V}{11.7\text{mohm}} = 85.47\text{A} \).

**Line 2**

The \( I_{DM} \) is defined by Pulsed Drain Current of datasheet. It is based on the \( I_D @ T_C \) 25°C value and generally speaking, \( I_{DM} = 4 \times I_D(@T_C \text{ 25°C}) \)

\[
I_D = \sqrt{\frac{T_J - T_C}{R_{BJC} \times K \times R_{DS(on)}}} \quad @25°C
\]

**Line 3**

This line is limited by the breakdown voltage.

**Line 4**

This line is limited by the a lot of parameters, including \( T_J, T_C, P_D, R_{BJC}, Z_{BJC} \), and \( K \) factor \( (R_{DS(on)} \) vs. \( T_J \)). The normalized effective transient thermal impedance \( (Z_{BJC}) \) depends on different square wave pulse duration(t) then got the both \( P_D \) and \( I_D \) from below equation.

For example, take TSC 30V MOSFET as example:

\[ V_{DS} = 30V, R_{BJC} \text{ is } 3.8^\circ C/W, Z_{BJC} \text{ is } 0.31@1\text{mS} \]
\[ P_D = \frac{T_J - T_C}{R_{\text{thJC}} \times Z_{\text{thJC}}} \]
\[ I_D = \frac{P_D}{V_{DS}} \]

\[ P_D = \frac{(150^\circ \text{C} - 25^\circ \text{C})}{(3.8^\circ \text{C/W} \times 0.31)} = 106.11 \text{W} \quad I_D = \frac{106.11 \text{W}}{30 \text{V}} = 3.54 \text{A} \]

So, @1ms pulse and 30V condition, suggested operating current will not be exceeding 3.54A.

\[ K \text{ is } 1.85 \text{ @ } 150^\circ \text{C} \text{ - (Please refer to spec)} \]
\[ R_{\text{DS(on)}} \text{ is } 11.7 \text{mohm} \]

\[ I_D = \sqrt{\frac{T_J - T_C}{R_{\text{thJC}} \times K \times R_{\text{DS(on)}} \times Z_{\text{thJC}}}} \]
\[ V_{DS} = \frac{P_D}{I_D} \]

\[ I_D = \sqrt{\frac{150^\circ \text{C} - 25^\circ \text{C}}{3.8^\circ \text{C/W} \times 0.31 \times 1.85 \times 11.7 \text{mohm}}} = 70.02 \text{A @ 1ms} \]

\[ V_{DS} = \frac{106.11 \text{W}}{70.02 \text{A}} = 1.515 \text{V (Corner voltage @1ms condition)} \]

**Normalized Thermal Transient Impedance, Junction-to-Case**

Above picture provides the normalized effective transient thermal impedance. These curves can be Junction to Ambient or Case based. From above, TSC 30V MOSFET is based on junction to case condition. As the duty cycle and the pulse duration increase, the transient thermal impedance gets close to 1. In the other words, It approaches to steady state thermal resistance.

\[ T_J = T_C + P_{DM} \times Z_{\text{thJC}} \times R_{\text{thJC}} \]

For example, the TSM120NA03CR run in single pulse condition, the \( Z_{\text{thJC}} \) based on curve is 0.31 at 1ms. The \( R_{\text{thJC}} \) is 3.8°C/W and \( P_{DM} \) is 1.5W. So the junction temperature of TSM120NA03CR at \( T_C=100^\circ \text{C} \) can be got as below list.

\[ T_J = 100^\circ \text{C} + 1.5 \text{W} \times 0.31 \times 3.8^\circ \text{C/W} = 101.767^\circ \text{C} \]
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